REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1, 2, 4, 5 and 7-11 are in this case. Claims 1, 2, 4, 5 and 7-11 have been rejected under § 103(a). Independent claims 1 and 4 have been amended. New claims 12 and 13 have been added.

The claims before the Examiner are directed toward a system and method for recording data in a multi-board solid-state storage system. The system includes a main board and several memory boards, each of which boards has primary and secondary non-volatile memory. The secondary memory of each board is used to store records of faulty locations of the board's primary memory.

§ 103(a) Rejections – Ajanovic '426 in view of Jeddeloh '798 and further in view of Okaue et al. '140

The Examiner has rejected claims 1, 2, 4, 5, 7 and 8 under § 103(a) as being unpatentable over Ajanovic, US Patent No. 6,298,426 (henceforth, "Ajanovic '426") in view of Jeddeloh, US Patent No. 6,052,798 (henceforth, "Jeddeloh '798") and further in view of Okaue et al., US Patent No. 6,601,140 (henceforth, "Okaue et al. '140"). The Examiner's rejection is respectfully traversed.

Ajanovic '426 teaches a computer system whose main memory **106** includes four (Figure 2) or three (Figure 3) volatile memory modules (DIMMs) **200** or **300** that plug into the motherboard. Each memory module includes a nonvolatile NVRAM **201** or **301** for storing information about the memory module such as (column 3 lines 65-66):

...memory data width, ECC, memory size, DRAM or SDRAM.

Jeddeloh '798 teaches a computer system **10** that includes a memory module **12**. Memory module **12** has a volatile memory block **14** and a nonvolatile memory block **16** that stores a map **18** of defective portions of volatile memory block **14**.

Applicant acknowledges that it is obvious from Ajanovic '426 and Jeddeloh '798 to associate a respective non-volatile memory with each volatile memory of a system that includes more than one volatile memory (as in Ajanovic '426) and to store in each such non-volatile memory a record of the faulty locations of the associated volatile memory (as in Jeddeloh '798).

Okaue et al. '140 teach a digital audio recorder/player **1** and associated memory cards **40** and **40'** that are reversibly attachable to digital audio recorder/player 1. Each memory card **40** and **40'** includes a flash memory **42**. Each memory card **40** also includes a security block **52** that enables memory card **40** to restrict access to the data stored in its flash memory **42**. For this purpose, security block **52** includes a non-volatile memory **55** for storing a decryption/storage key.

The Examiner cites Okaue et al. '140 to show that it is known in the art to associate a secondary non-volatile memory (non-volatile memory **55**) with a primary non-volatile memory (flash memory **42**). The Examiner proposes that it then is obvious to substitute non-volatile memory modules for volatile memory modules **200** or **300** of Ajanovic '426, thereby obtaining the present invention as recited in independent claims 1 and 4.

Actually, all that is obvious from Ajanovic '426, Jeddeloh '798 and Okaue et al. '140 is to store in non-volatile memory **55** of Okaue et al. '140 a record of the faulty locations of flash memory **42** of Okaue et al. '140. It would not have been obvious from these references, to one ordinarily skilled in the art, to substitute non-volatile memory modules for volatile memory modules **200** or **300** of Ajanovic '426,

because the purpose served by volatile memory modules **200** or **300** of Ajanovic '426 is quite different from the purpose served by memory cards **40** of Okaue et al. '140. Memory cards **40** of Okaue et al. '140 are for securely storing audio data, for example copyrighted music. A user of digital audio recorder/player **1** of Okaue et al. '140 typically attaches one and only one memory card **40** at a time to serial interface **11** of digital audio recorder/player **1** in order to listen to the audio data stored in that memory card **40**. When that user is finished listening to the audio data on a memory card **40**, s/he typically detaches that memory card **40** from digital audio recorder/player **1** and replaces it with a different memory card **40**. That user even has the option of attaching an insecure memory card **40'**, that lacks security block **52** and the associated non-volatile memory **55**, into digital audio recorder/player **1** in place of memory card **40**. By contrast, main memory **106** of the computer system of Ajanovic '426 typically includes several memory modules **200** or **300** (for example, four memory modules **200** as illustrated in Figure 2 or three memory modules **300** as illustrated in Figure 3) that cooperate collectively with memory controller **104** of main memory **106**. Memory modules **200** or **300** typically remain plugged into the motherboard together until the computer system needs to be repaired or upgraded. One ordinarily skilled in the art therefore would not think of memory cards **40** of Okaue et al. '140 and memory modules **200** or **300** of Ajanovic '426 as interchangeable. Any assertion to the contrary constitutes impermissible hindsight on the part of the Examiner.

The Examiner has cited the desire of Ajanovic '426, as stated in column 3 lines 34-40, to have compatibility with different types of memory modules, in support of the alleged obviousness of substituting non-volatile memory modules for volatile memory modules **200** or **300**. In fact, this desire provides no such support because all

of the alternative memory modules listed in that citation (SIMM modules, MCMs, etc.) are volatile memory modules.

The Examiner also has cited column 3 lines 41-45 of Jeddeloh '798 as teaching the alternate use of a volatile memory or a nonvolatile memory for the same purpose. This citation is not relevant to the present invention because the memory in question, memory **38** of memory controller **20**, is used to store a copy **18A** of map **18**. Memory **38** therefore corresponds to the secondary non-volatile memory devices of the present invention, and not to the primary memory devices of the present invention. The issue before the Examiner is whether it is obvious from the cited references to make the primary memory devices of the present invention non-volatile.

Conceivably, independent claim 1 could be construed as reading on one configuration of the obvious combination of the cited references: digital audio recorder/player **1** of Okaue et al. '140 with a memory card **40** attached to interface **11** and with a record of the faulty locations of flash memory **42** of that memory card **40** stored in non-volatile memory **55** of that memory card **40**. Therefore, to make sure that the invention recited in independent claim 1 is patentably distinct from the obvious combination of the cited references, independent claim 1 has been amended to recite a plurality of memory boards. As best understood, only one memory card **40** at a time would ever be attached to digital audio recorder/player **1** because the user of digital audio recorder/player **1** could listen to only one audio file at a time. Support for this amendment is found in Figure 3 that shows three memory boards.

With independent claim 1 allowable in its present form, it follows that claims 2 and 7, that depend therefrom, also are allowable.

Although claim 2 is allowable merely by virtue of depending from claim 1, Applicant respectfully directs the Examiner's attention to an additional reason for the

allowability of claim 2. Claim 1 states that the memory boards are separate from the main board. Now, the Examiner has construed memory controller **104** of Ajanovic '426 as corresponding to the main board of the present invention. In that case, memory modules **200** or **300** of Ajanovic '426, that are separate from memory controller **104**, correspond only to the memory boards of the present invention. There is neither a hint nor a suggestion in Ajanovic '426 of including both primary and secondary memory, whether volatile or nonvolatile, in memory controller **104**.

Independent claim 4 also has been amended to preclude reading on the obvious combination of the cited references. Specifically, the preamble of independent claim 4 has been amended to recite the configuration now recited in independent claim 1: a main board and a plurality of memory boards, with the main board including a processing system for enabling interaction with a host system. Support for this amendment is found in Figure 3. For further consistency with independent claim 1, which requires the presence of the secondary non-volatile memory devices only on the memory boards, independent claim 4 also has been amended to require placing primary and secondary non-volatile memories, and recording the faulty locations of the primary memories in the secondary memories, only in the memory boards. Support for this broadening of independent claim 4 is found in independent claim 1 as filed. The limitations that primary and secondary memories are placed also on the main board, and that the faulty locations of the main board's primary memory are recorded in the main board's secondary memory, now have been re-introduced in new claim 13.

With independent claim 4 allowable in its present form, it follows that claims 5 and 8, that depend therefrom, also are allowable.

§ 103(a) Rejections – Ajanovic '426 in view of Jeddeloh '798 and further in view of Gross et al. '959

The Examiner has rejected claims 9-11 under § 103(a) as being unpatentable over Ajanovic '426 in view of Jeddeloh '798 and further in view of Gross et al., US Patent No. 5,200,959 (henceforth, "Gross et al. '959"). The Examiner's rejection is respectfully traversed.

Gross et al. '959 teach a flash memory array **100** that includes a static information list **120**, a dynamic information list **130** and a user data portion **110**. After flash memory array **100** is manufactured, its initial defects are recorded in static information list **120**. As data are written to user data portion **110**, defects that arise subsequently during the use of flash memory array **100** are recorded in dynamic information list **130**.

The crucial difference between the present invention, as recited in independent claim 9, and the teachings of Gross et al. '959, is that Gross et al. '959 record each defect only once. By contrast, independent claim 9 requires that at least one faulty location record be recorded at least twice, in each of at least two areas of the relevant secondary non-volatile memory device. Therefore, Gross et al. '959 is not relevant to the present invention as recited in independent claim 9.

With independent claim 9 allowable in its present form, it follows that claims 10 and 11, that depend therefrom, also are allowable.

Other New Claims

As noted above, the support for the limitation now introduced to independent claim 1, that the system of the present invention includes a plurality of memory boards, lies in Figure 3. Figure 3, that illustrates a system with three memory boards, provides explicit support for a system that includes three memory boards, and not just

two memory boards. Therefore, new claim 12 has been added. New claim 12 requires the system of claim 1 to have at least three memory boards. Support for new claim 12 is found in Figure 3. New claim 12 is allowable by virtue of depending from independent claim 1.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 4 and 9, and hence dependent claims 2, 5, 7, 8 and 10-13 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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